PATENT
Docket No.: FOV-155

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2826 Examiner: Ahmen D. Sefer

Serial No. 10/796,763 Filed: March 8, 2004

In re Application of: Hynecek et al.

For: METHOD AND APPARATUS FOR IMPROVING SENSITIVITY IN VERTICAL COLOR CMOS IMAGE SENSORS

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail, in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on January 30, 2006.

Signed Carri Chandler

Name

DECLARATION OF RICHARD B. MERRILL

I, Richard B. Merrill, declare and state as follows:

1. I am employed by Foveon, Inc., the assignee of the above-identified patent application. I obtained my BSEE from Dartmouth College in 1978. I was employed by IBM as an engineer from 1978 until 1981. I was employed by National Semiconductor Corporation as a staff engineer from 1981 through 1996, when I joined the staff at Foveon. I have been involved in the design of integrated circuits and the semiconductor devices they contain since 1978. As a result of my education and experience, I consider myself to be a person of ordinary skill in the art of integrated circuit and device design.

2. I am the inventor of the subject matter disclosed and claimed in the above-identified patent application. I am familiar with and understand the contents of the above-identified patent application.

3. I am also the inventor of the subject matter disclosed and claimed in United States Patent No. 6,930,336. I am familiar with and understand the content of United States Patent No. 6,930,336.

4. I have read and understood the Office Action in the above-identified patent application that was mailed on September 30, 2005.

5. The Examiner asserts that United States Patent No. 6,930,336 discloses a CMOS image sensor comprising (among other things) "a first doped charge collecting region 46 buried within the p-type doped region and configured to operate as a depleted potential well." The Examiner's assertion is incorrect. The charge collecting region 46 buried within the p-type doped region in the CMOS image sensor disclosed in United States Patent No. 6,930,336 is not configured to operate as a depleted potential well as required by claim 1 of the above-identified patent application. Collecting region 46 in United States Patent No. 6,930,336 does not operate as a depleted potential well. In order for collecting region 46 to operate as a depleted potential well, the disclosure of the reference would have to

be modified. The voltage on collecting region 46 would have to be increased from what is disclosed to a value that would cause the image sensor to operate in a substantially degraded fashion with unacceptable leakage. Because of this problem that would result from such operation, it is my opinion that no person of ordinary skill in the art would be motivated to modify the disclosure of United States Patent No. 6,930,336 to operate this device in that fashion.

6. The Examiner also asserts that the admitted prior art disclosed with reference to FIG. 1 of the above-identified patent application discloses a CMOS image sensor comprising (among other things) "a first doped charge collecting region 103 buried within the p-type doped region and configured to operate as a depleted potential well." The Examiner's assertion is incorrect. The charge collecting region 103 buried within the p-type doped region 102 in the CMOS image sensor as disclosed in FIG. 1 of the above-identified patent application is not configured to operate as a depleted potential well as required by claim 1 of the above-identified patent application. FIG. 1 of the above-identified patent application discloses the structure of prior imaging sensors that were manufactured by Foveon, the assignee of the present invention. The image sensor depicted in FIG. 1 of the above-identified patent application does not operate in that manner wherein collecting region 103 operates as a depleted potential well.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.

Richard B. Merrill

1-27-06
Date